DETAILED ACTION

Claim Objections

1.   **Claims 1 and 22** are objected to because of the following informalities: in the

limitation: "a pointer in a shift register for determining which rows of the matrix are to be

enabled for **talking** part in the data transfer of all of the data items of the data word", the

applicant uses the word "talking" where it should be "taking" based upon previous claim

language. Appropriate correction is required.

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed
> or described as set forth in section 102 of this title, if the differences between the
> subject matter sought to be patented and the prior art are such that the subject
> matter as a whole would have been obvious at the time the invention was made
> to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was
> made.

2.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating
        obviousness or nonobviousness.

3.   **Claims 1-2, 4-6, 10, 12-13, 18-19, 21-23 and 25** are rejected under 35

U.S.C. 103(a) as being unpatentable over Baddiley (US 4,852,065), and further in view

of Anderson et al. (US 2004/0111567), Kim et al. (US 6,781,898 B2) and Glover (US
5,581,773).

4.   Consider **claim 1**, Baddiley discloses a multi-ported orthogonal data memory for
effecting a corner-turning function, where for example data input as a sequence of bit-
parallel word-serial data transfers are converted to data output in a bit-serial, word-
parallel fashion; the memory being arranged to transfer data words comprising a
plurality of data items (fig. 2, abstract, Col. 1 lines 4-30 and Col. 3 lines 20-50, where a
data item is considered to be a data word or some portion of a data word.) and
comprising: a plurality of data memory cells arranged in the form of a matrix having
rows and columns, wherein the memory further comprises a plurality of different and
non-sequential groups of memory cells within the matrix (fig. 2, where the
reorganization unit of fig. 2 is considered the memory, each buffer of the memory is in
the form of a matrix with rows and columns and a plurality of different and non-
sequential groups of memory cells is considered buffers 20 and 21.), each group being:
i) a subgroup of the total number of memory cells in the matrix (fig. 2, where each buffer
is a subgroup of the total number of memory cells in the matrix.), ii) having members of
the group located in different rows and in different columns of the matrix (fig. 2, Col. 3
lines 20-58, where each bit position is considered a member and each one is located
across different rows and columns that make up each buffer.), and iii) being individually
addressable to effect transfer of a data word thereto (fig. 2, Col. 3 lines 20-58, Each
RAM component of each buffer contains 512 individually addressable locations); and
enabling means having dedicated strobe connections to each of the plurality of groups

of memory cells and being arranged to exclusively enable memory cells belonging to a selected ones of the plurality of groups, as determined by the size of the data items being transferred, to read all of the data items of the data word present at their inputs into the selected group of memory cells or to write all of the data items of the data word stored in the selected group of memory cells to their outputs in a single transfer operation (Fig. 2 and 3, Col. 3 lines 20-58 and Col. 5 lines 1-10, where each buffer, and the number of addressable locations within the buffer, is selected after a determination of/based on the size of the data items is made and the arrangement of the data in the buffer is effected by the word size. Each buffer has dedicated connections for reading out and writing in data words as shown in fig. 2 and 3 and a write or read operation is considered a single transfer operation.), **the enabling means being arranged to enable a selected group upon a set of logic conditions becoming true, the logic conditions being determined from a current selected row of the matrix and the size of the items being transferred** (Baddiley: fig. 2 and 4, Col. 3 lines 20-59 and Col. 5 lines 1-10, where logic conditions include the decoder using the control and address bits to select particular rows or columns in a particular buffer), **the enabling means comprises: selection means for selecting the current size of the data items in the data word and configuring the enabling means to operate with the selected current size of data items** (Baddiley: Col. 5 lines 1-10, where the size of the data items in the word is considered the size of the data items together that make up the whole word); **byte column determining means for enabling a specific group of byte column locations of the matrix within a selected word row to be enabled for**

transferring an item of the data word across a word port of the memory (Baddiley:

Fig. 3-4 Col. 4 lines 6-46 and Col. 5 lines 45-62, where register 46 comprises a

reference to counter 41 and is used in determining the control and address bits to

enable particular columns of the matrix and 43 determines which buffer is being

referenced by which register/counter combination**), the byte column determining

means comprises a first table specifying the relationship between the plurality of

different groups of memory cells and their respective memory cell locations in

the matrix** (Baddiley: fig. 3-4, Col. 3-4 lines 29-41 and 59-33 and Col. 5 lines 45-62,

where register's 40 and 41 consist of a linear table of bits with indicate a particular

row/column for reading or writing information in a particular buffer); **bit column

determining means for enabling a specific group of bit column locations of the

matrix within a selected word row to be enabled for transferring a bit of an item of

the data word across a bit port of the memory** (Baddiley: Fig. 3-4 Col. 4 lines 6-46

and Col. 5 lines 45-62, where register 46 comprises a reference to counter 41 and is

used in determining the control and address bits to enable particular columns of the

matrix and 43 determines which buffer is being referenced by which register/counter

combination), **the bit column determining means comprises a second table

specifying the relationship between the plurality of different groups of memory

cells and their respective memory cell locations in the matrix** (Baddiley: fig. 3-4,

Col. 3-4 lines 29-41 and 59-33 and Col. 5 lines 45-62, where register's 40 and 41

consist of a linear table of bits with indicate a particular row/column for reading or writing

information in a particular buffer); **and a pointer in a shift register for determining**

which rows of the matrix are to be enabled for taking part in the data transfer of

all of the data items of the data word (Baddiley: Fig. 4, Col. 3 lines 50-59, Col. 4 lines

33-37, where register 45 comprises a reference to counter 40 and is used in

determining the control and address bits to enable particular rows of the matrix).

Baddiley does not explicitly disclose that the claimed single transfer operation

occurs in a single clock cycle. But Anderson et al. does teach that it is conventional for a

multi-port memory devices to be able to read and write data in a single clock cycle (pg.

1 ¶ [0010]) and further that the improved multiport-memory of Anderson can also

perform read and write access operations in one clock cycle, this improved multiport-

memory can provide a significant reduction in chip area for a given memory storage

capacity.

It would have been obvious to one of ordinary skill in the art at the time of the

invention for the multi-ported memory of Baddiley to be able to perform read and write

operations in one clock cycle, because Anderson et al. teaches that conventional multi-

port memories can perform read and write accesses to data in one clock cycle (pg. 1 ¶

[0010]) and further because the improved multiport-memory of Anderson can also

perform read and write access operations in one clock cycle, this improved multiport-

memory can provide a significant reduction in chip area for a given memory storage

capacity (pg. 1 ¶'s [0010] and [0011]).

Baddiley in view of Anderson et al. do not disclose what happens if a faulty row

exists in the matrix, however Kim et al. does teach the following claimed features:

means for storing information relating to a faulty row in the matrix and wherein

the shifting word pointer register is arranged to be controlled to skip the faulty

row in the matrix and instead point to otherwise redundant additional row of the

matrix (abstract, Col. 1 lines 40-46 and Col. 2 lines 8-23).

It would have been obvious to one of ordinary skill in the art at the time of the

invention to include the teachings of Kim et al. with that of Baddiley and Anderson et al.,

because Kim teaches that detecting and skipping defective rows in a memory and then

using an additional redundant row in its place, doing this improves memory yield and

ensures proper operation of the memory (abstract, Col. 1 lines 23-46 and Col. 2 lines 8-

23).

Baddiley in view of Anderson et al. and Kim et al. do not discuss the use of a

mask register, however Glover does disclose the claimed features of: **a first masking**

register arranged to mask bits of the data to be read out of the matrix of memory

cells via a bit port of the memory (Col. 4 lines 11-14 and 65-67 and Col. 10 lines 57-

62).

It would have been obvious to one of ordinary skill in the art at the time of the

invention to include the teachings of Glover with that of Baddiley in view of Anderson et

al. and Kim et al., because Glover teaches that using the PE's and register's in the

manner discloses can exclude the need for special corner turning hardware and allow

for more PE's per chip therefore yielding significantly greater implementation economies

and reduce cost and complexity (Col. 1 lines 43-55 and Col. 2 lines 37-67).

5.   Consider **claim 22**, Baddiley disclose a multi-ported orthogonal data memory for

effecting a data corner-turning function between a plurality of processors and location

addressable data store, the memory being arranged to transfer input data words
comprising a plurality of data items across a word port for the data store and transfer
data bits comprising an output word across a bit port for the processors (fig. 2, abstract,
Col. 1 lines 4-30 and Col. 3 lines 20-50, where a data item is considered to be a data
word or some portion of a data word.), the memory comprising: a plurality of data
memory cells arranged in the form of a matrix having rows and columns, wherein the
memory further comprises a plurality of different and non-sequential groups of memory
cells within the matrix (fig. 2, where the reorganization unit of fig. 2 is considered the
memory, each buffer of the memory is in the form of a matrix with rows and columns
and a plurality of different and non-sequential groups of memory cells is considered
buffers 20 and 21.), wherein each group: i) a subgroup of the total number of memory
cells in the matrix (fig. 2, where each buffer is a subgroup of the total number of memory
cells in the matrix.), ii) having members of the group located in different rows and in
different columns of the matrix (fig. 2, Col. 3 lines 20-58, where each bit position is
considered a member and each one is located across different rows and columns that
make up each buffer.), iii) relates to a different size of data item (fig. 2, Col. 3 lines 20-
58 and Col. 5 lines 1-10, each group can be used to handle words of 32-bit size or
smaller based on preset values and therefore each group is related to data items of a
different size.) and iv) is individually addressable to effect transfer of a data word thereto
(fig. 2, Col. 3 lines 20-58, Each RAM component of each buffer contains 512 individually
addressable locations); and enabling means having dedicated strobe connections to
each of the plurality of groups of memory cells and being arranged to exclusively enable

memory cells belonging to a selected ones of the plurality of groups, as determined by the size of the data items being transferred, to transfer all of the data items of the input data word via the word port into the selected group or bit data representing an output data word stored in the selected group via the bit port in a single transfer operation (Fig. 2 and 3, Col. 3 lines 20-58 and Col. 5 lines 1-10, where each buffer, and the number of addressable locations within the buffer, is selected after a determination of/based on the size of the data items is made and the arrangement of the data in the buffer is effected by the word size. Each buffer has dedicated connections for reading out and writing in data words as shown in fig. 2 and 3 and a write or read operation is considered a single transfer operation.), **the enabling means being arranged to enable a selected group upon a set of logic conditions becoming true, the logic conditions being determined from a current selected row of the matrix and the size of the items being transferred** (Baddiley: fig. 2 and 4, Col. 3 lines 20-59 and Col. 5 lines 1-10, where logic conditions include the decoder using the control and address bits to select particular rows or columns in a particular buffer), **the enabling means comprises: selection means for selecting the current size of the data items in the data word and configuring the enabling means to operate with the selected current size of data items** (Baddiley: Col. 5 lines 1-10, where the size of the data items in the word is considered the size of the data items together that make up the whole word); **byte column determining means for enabling a specific group of byte column locations of the matrix within a selected word row to be enabled for transferring an item of the data word across a word port of the memory** (Baddiley: Fig. 3-4 Col.

4 lines 6-46 and Col. 5 lines 45-62, where register 46 comprises a reference to counter 41 and is used in determining the control and address bits to enable particular columns of the matrix and 43 determines which buffer is being referenced by which register/counter combination), **the byte column determining means comprises a first table specifying the relationship between the plurality of different groups of memory cells and their respective memory cell locations in the matrix** (Baddiley: fig. 3-4, Col. 3-4 lines 29-41 and 59-33 and Col. 5 lines 45-62, where register's 40 and 41 consist of a linear table of bits with indicate a particular row/column for reading or writing information in a particular buffer); **bit column determining means for enabling a specific group of bit column locations of the matrix within a selected word row to be enabled for transferring a bit of an item of the data word across a bit port of the memory** (Baddiley: Fig. 3-4 Col. 4 lines 6-46 and Col. 5 lines 45-62, where register 46 comprises a reference to counter 41 and is used in determining the control and address bits to enable particular columns of the matrix and 43 determines which buffer is being referenced by which register/counter combination), **the bit column determining means comprises a second table specifying the relationship between the plurality of different groups of memory cells and their respective memory cell locations in the matrix** (Baddiley: fig. 3-4, Col. 3-4 lines 29-41 and 59-33 and Col. 5 lines 45-62, where register's 40 and 41 consist of a linear table of bits with indicate a particular row/column for reading or writing information in a particular buffer); **and a pointer in a shift register for determining which rows of the matrix are to be enabled for taking part in the data transfer of all of the data items of the data word**

(Baddiley: Fig. 4, Col. 3 lines 50-59, Col. 4 lines 33-37, where register 45 comprises a reference to counter 40 and is used in determining the control and address bits to enable particular rows of the matrix).

Baddiley does not explicitly disclose that the claimed single transfer operation occurs in a single clock cycle. But Anderson et al. does teach that it is conventional for a multi-port memory devices to be able to read and write data in a single clock cycle (pg. 1 ¶ [0010]) and further that the improved multiport-memory of Anderson can also perform read and write access operations in one clock cycle, this improved multiport-memory can provide a significant reduction in chip area for a given memory storage capacity.

It would have been obvious to one of ordinary skill in the art at the time of the invention for the multi-ported memory of Baddiley to be able to perform read and write operations in one clock cycle, because Anderson et al. teaches that conventional multi-port memories can perform read and write accesses to data in one clock cycle (pg. 1 ¶ [0010]) and further because the improved multiport-memory of Anderson can also perform read and write access operations in one clock cycle, this improved multiport-memory can provide a significant reduction in chip area for a given memory storage capacity (pg. 1 ¶'s [0010] and [0011]).

Baddiley in view of Anderson et al. do not disclose what happens if a faulty row exists in the matrix, however Kim et al. does teach the following claimed features: **means for storing information relating to a faulty row in the matrix and wherein the shifting word pointer register is arranged to be controlled to skip the faulty**

row in the matrix and instead point to otherwise redundant additional row of the

matrix (abstract, Col. 1 lines 40-46 and Col. 2 lines 8-23).

It would have been obvious to one of ordinary skill in the art at the time of the

invention to include the teachings of Kim et al. with that of Baddiley and Anderson et al.,

because Kim teaches that detecting and skipping defective rows in a memory and then

using an additional redundant row in its place, doing this improves memory yield and

ensures proper operation of the memory (abstract, Col. 1 lines 23-46 and Col. 2 lines 8-

23).

Baddiley in view of Anderson et al. and Kim et al. do not discuss the use of a

mask register, however Glover does disclose the claimed features of: **a first masking**

register arranged to mask bits of the data to be read out of the matrix of memory

cells via a bit port of the memory (Col. 4 lines 11-14 and 65-67 and Col. 10 lines 57-

62).

It would have been obvious to one of ordinary skill in the art at the time of the

invention to include the teachings of Glover with that of Baddiley in view of Anderson et

al. and Kim et al., because Glover teaches that using the PE's and register's in the

manner discloses can exclude the need for special corner turning hardware and allow

for more PE's per chip therefore yielding significantly greater implementation economies

and reduce cost and complexity (Col. 1 lines 43-55 and Col. 2 lines 37-67).

Baddiley uses an array of processing elements, but does not explicitly disclose

whether these processing elements are SIMD processors, however Glover does teach

the use of an array of processing elements just like in Baddiley that utilize SIMD

processors (Col. 1 lines 13-55 and Col. 2 lines 28-42)

It would have been obvious to one of ordinary skill in the art at the time of the

invention to include the teachings of Glover with that of Baddiley, because Glover

teaches that SIMD processors are frequently used to process image data, just as the

processor array in Baddiley is designed to do, therefore being a common and well-

known (Col. 1 lines 41-43).

6.   Consider **claim 2**, Baddiley in view of Anderson et al., Kim et al. and glover

discloses a memory according to **Claim 1**, wherein each of the groups of memory cells

is specified according to its use in transferring the data items of the data word to or from

the matrix to effect the corner-turning function (Baddiley: Col. 3 lines 20-58, each buffer

is designated to either be a write or read buffer).

7.   Consider **claim 4**, Baddiley in view of Anderson et al., Kim et al. and glover

discloses a memory according to **Claim 1**, wherein the number of different groups of

memory cells provided within the matrix equals the number of different sizes of data

items which can be handled by the memory (Baddiley: Fig. 2, col. 3 lines 20-50 and Col.

5 lines 1-10, where a group of memory cells can be considered any subset of memory

cells of a buffer that spans multiple rows and columns and word sizes of 32 bits or lower

can be used by the system, therefore since a group is merely defined as spanning

multiple rows and columns, the number of groups can be equal to the number of sizes

available).

8.   Consider **claim 5**, Baddiley in view of Anderson et al., Kim et al. and glover
discloses a memory according to **Claim 1**, wherein each item of the data word being
transferred is an integer power-of-two multiple of eight bits (Baddiley: Col. 5 lines 1-10).

9.   Consider **claim 6**, Baddiley in view of Anderson et al., Kim et al. and glover
discloses a memory according to **Claim 1**, wherein the memory is arranged to operate
with different types of data words, each type comprising 64, 32, 16 or 8-bit data items
(Baddiley: Col. 5 lines 1-10).

10.   Consider **claim 10**, Baddiley in view of Anderson et al., Kim et al. and glover
discloses a memory according to **Claim 1**, wherein the pointer in the shift register (38)
is configured to be operable in a plurality of different modes , each mode corresponding
to a possible size of the data item being transferred, the pointer being configured within
a single instruction to advance by a predetermined number of bit positions as
determined by the current mode thereby indicating which rows of the matrix are to be
enabled to facilitate transfer of the whole of the data word to or from the matrix
(Baddiley: fig. 4, Col. 3 lines 30-59, col. 4 lines 33-37 and Col. 5 lines 1-10, where
register 45 determines word size and address and control bits to indicate rows and
columns of a matrix to facilitate transfer of data words).

11.   Consider **claim 12**, Baddiley in view of Anderson et al., Kim et al. and glover
discloses a memory according to **Claim 1**, further comprising means for converting the
current position of the row pointer in the shift register (38) to one or more row select
logic signals (Baddiley: Fig. 4, Col. 3 lines 50-59, Col. 4 lines 33-37, where register 45

comprises a reference to counter 40 and is used in determining the control and address bits to enable particular rows of the matrix).

12.   Consider **claim 13**, Baddiley in view of Anderson et al., Kim et al. and glover discloses a memory according to **Claim 12**, further comprising a hard-wired backward propagation network for determining, from the bit position of the pointer and the size of the current data items, the rows of the matrix that are to be enabled for the data transfer (Baddiley: Fig. 4, Col. 3 lines 50-59, Col. 4 lines 33-37, where register 45 comprises a reference to counter 40 and is used in determining the control and address bits to enable particular rows of the matrix, the components of fig. 4 perform the functions claimed to be performed by the hard-wired backward propagation network).

13.   Consider **claim 18**, Baddiley in view of Anderson et al., Kim et al. and glover discloses a memory according to **Claim 1**, wherein the locations of the memory cells of each group form a repeating pattern when viewed as a matrix (Baddiley: fig. 2).

14.   Consider **claim 19**, Baddiley in view of Anderson et al., Kim et al. and glover discloses a memory according to **Claim 1**, further comprising a load register (42) arranged to retain temporarily bit-serial word parallel data transferred to and from the matrix of memory cells across a bit port of the memory (Baddiley: Fig. 3 and Col. 4 lines 20-25).

15.   Consider **claim 21**, Baddiley in view of Anderson et al., Kim et al. and glover discloses a memory according to **Claim 1**, further comprising a second masking register arranged to mask bits of the data to be input to the matrix of memory cells via a bit port of the memory (Glover: Col. 4 lines 11-14 and 65-67 and Col. 10 lines 57-62).

16.   Consider **claim 23**, as applied to **claim 22** above, Baddiley in view of Anderson et al., Kim et al. and glover disclose further comprising a plurality of SIMD associative processors (Glover: Col. 1 lines 13-55 and Col. 2 lines 28-42)

17.   Consider **claim 25**, Baddiley in view of Anderson et al., Kim et al. and glover discloses a memory according to **Claim 22**, wherein the enabling means comprises a pointer in a shift register (38) for determining which rows of the matrix are to be enabled for taking part in the data transfer of all of the data items of the data word (Baddiley: Fig. 4, Col. 3 lines 50-59, Col. 4 lines 33-37, where register 45 comprises a reference to counter 40 and is used in determining the control and address bits to enable particular rows of the matrix).

Response to Arguments

18.   Applicant's arguments filed 1/30/2012 have been fully considered but they are not persuasive.

19.   The Applicant has moved previously rejected claim limitations into the independent claims and generally alleges that the new combination of rejected independent claim limitations along with previously rejected dependent claim limitations are not taught by the combination of references used by the Examiner. Thus, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

20.   The combination of limitations, now required by the independent claims, are considered to still be taught by the primary reference and the straight forward 103 rejections as presented previously when the limitations were separately claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-1182. The examiner can normally be reached on Monday through Thursday 9:00AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael Alsip

Primary Examiner
Art Unit 2186

/Michael Alsip/
Primary Examiner, Art Unit 2186

February 22, 2012